Powering Crusoe™ CPU with ISL6211

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Author: Vladimir A. Muratov

Introduction

The Crusoe™ family of x86 compatible processors combines strong performance with remarkably low power consumption. The new technology for designing microprocessors underlies the achievement. The new technology is fundamentally software based: the power savings come from replacing large numbers of transistors with software.

The Crusoe processor solutions consist of a hardware engine logically surrounded by a software layer. The engine is a very long instruction word (VLIW) CPU capable of executing up to four operations in each clock cycle. The software layer is called Code Morphing™ software because it dynamically “morphs” x86 instructions into VLIW instructions. The surrounding software layer gives x86 programs the impression that they are running on x86 hardware.

The Code Morphing™ software is a major, but not the only one contributor to power reduction. LongRun™ power management is another facility that further minimizes the processor's power. The LongRun™ software continuously monitors the demand on the processor and dynamically sets the right clock speed and core voltage needed to run the application.

All these advances in microprocessor architecture require adequate performance from the VRM.

The ISL6211 CPU core PWM controller fits especially well into the requirements specified by the Crusoe™ family processors operating in conjunction with LongRun™ technology. The controller can operate a synchronous buck converter on selectable 300kHz/600kHz frequency. The VID codes can be dynamically changed with a controlled slew rate that dramatically simplifies support of different generations of CPUs. The output voltage can be programmed in two ways, either by the VID code, or by using the analog reference input. The last feature significantly reduces the number of external components required to support START and DSX CPU modes.

For more information on ISL6211 features see the data sheet FN9043 [1].

Evaluation Board Overview

The ISL6211EVAL board presents itself as a flexible tool to evaluate performance of the CPU core regulator without involving a real CPU, Figure 1. The built-in CPU load emulator performs dynamic output voltage changes that simulate transitions between START, DSX, and two performance modes, Figure 2. The output voltage changes are synchronized with corresponding on-board load transitions.

The CPU emulator can be disabled by S1 (see Figure 1 and Table 3). In this case, the output voltage is set by the Performance 1 VID combination. The conveniently provided scope probe sockets allow for monitoring of the output voltage and the switching waveforms.

The PLL power supply is also placed on the evaluation board for testing and evaluation of the core voltage tracking circuit that powers clock PLL, Figure 3.

Quick Start Evaluation

Out Of The Box

The ISL6211EVAL comes in a “ready-to-test” state. The board comes equipped with several jumpers pre-populated for operation with the load emulator on. Use Table 1 for jumper description. Table 3 describes the S1 function.

NOTE: pre-populated positions are highlighted in bold.

Required Test Equipment

To fully test the ISL6211 chip functionality characterized by this Application Note, the follow equipment is needed:

- 4 channel oscilloscope with probes
- 1 electronic load
- 2 bench power supplies (0-5V, 0-24V @ > 2.5A)
- Precision digital multi-meters

TABLE 1. JUMPER FUNCTIONALITY

JUMPER #	STATE	FUNCTION
JP1	**POP**	Normal Operation
	NOP	Measure operating current I_{VCC}
JP2	**POP**	Enable hysteretic operation in DSX mode only
	NOP	Enables hysteretic mode control by SW2
JP3	**POP**	Engages external circuit for maximum voltage limiting
	NOP	Disconnects the circuit
JP4	**POP**	Connects CPU leakage simulating resistors to the output
	NOP	Disconnects leakage resistors for efficiency measurements

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CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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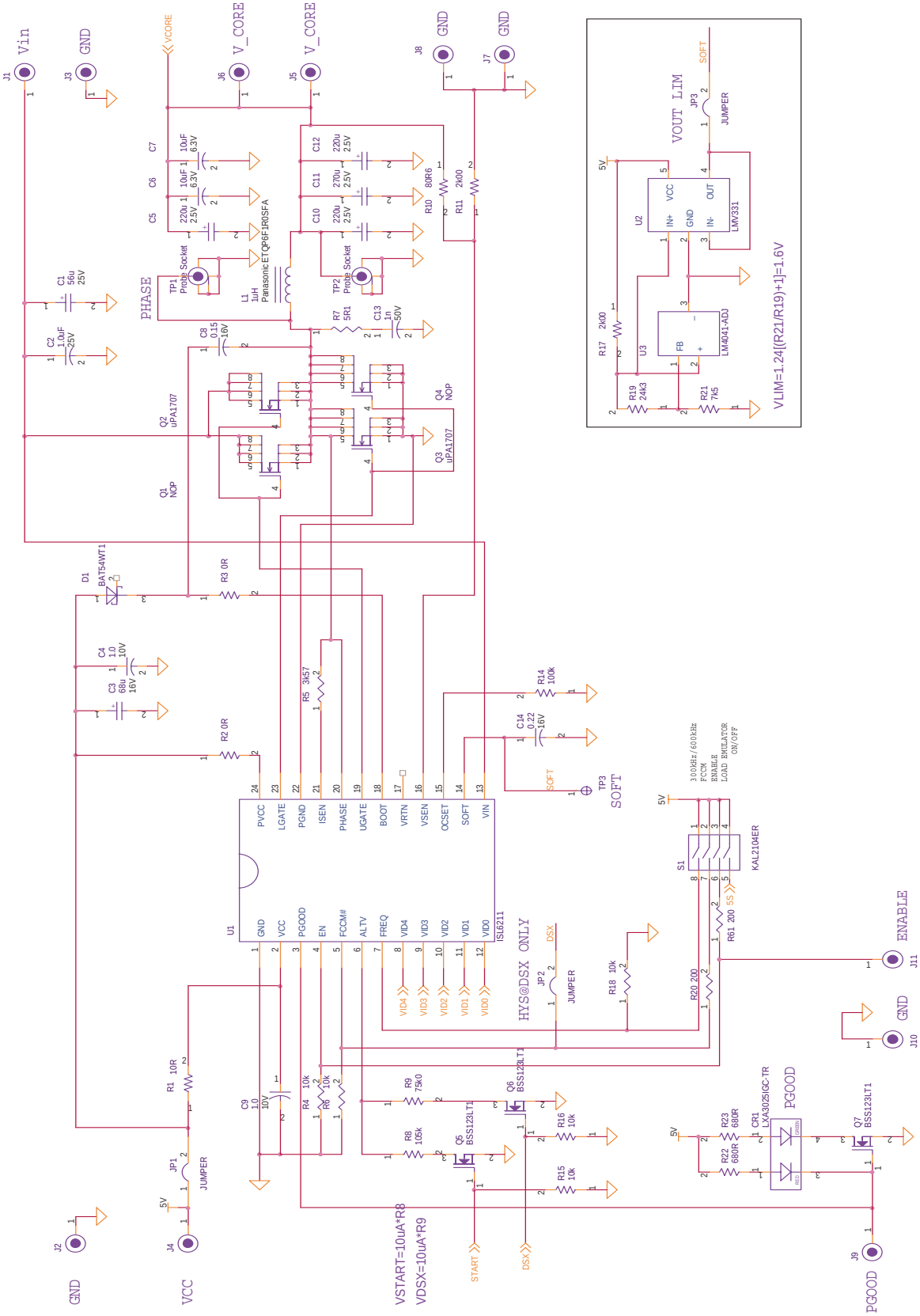

FIGURE 1. ISL6211 EVALUATION BOARD. DC_DC CONVERTER

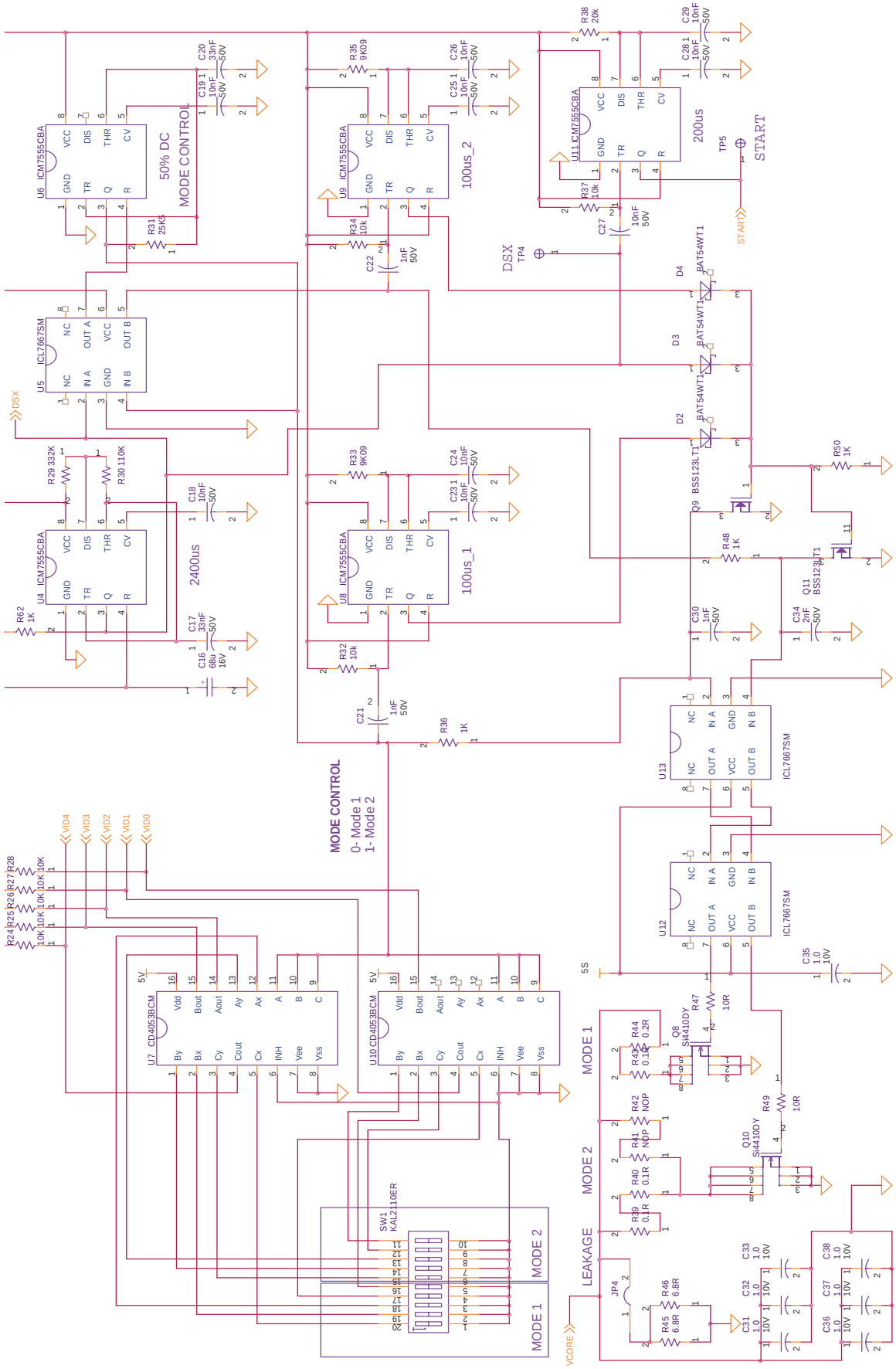

FIGURE 2. ISL6211 EVALUATION BOARD. CPU EMULATOR

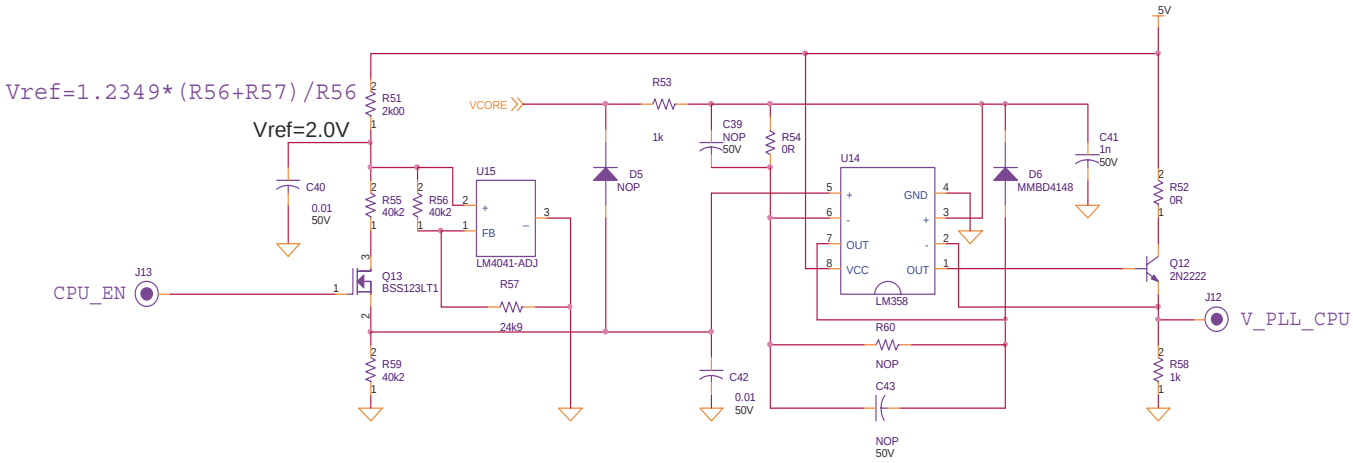

FIGURE 3. ISL6211 EVALUATION BOARD PLL POWER SUPPLY

TABLE 2. BILL OF MATERIALS

REFERENCE	DESCRIPTION	VENDOR	PART NO.	QTY
CR1	LED		LXA3025IGC-TR	1
C1	Capacitor 56µF	Sanyo OSCON	25SP56M	1
C2	Capacitor 10µF	Tayo Yuden	TMK432BJ106KM	1
C3, C16	Capacitor 68µF	Kemet	T494D686(1)016AS	1
C4, C9, C31, C32, C33, C35, C36, C37, C38	Capacitor 1.0µF	Kemet	C1206C105K8RAC	9
C5, C6, C7, C10, C11, C12	Capacitor 220µF	Sanyo POSCAP	2R5TPB220M	6
C8, C14	Capacitor 0.22µF	Kemet	C0805C224K4RAC	2
C13, C21, C22, C27, C30, C39, C41	Capacitor 1.0nF	Kemet	C0805C102K5RAC	7
C17, C20	Capacitor 33nF	Kemet	C0805C333K4RAC	2
C18, C19, C23, C24, C25, C26, C28, C29, C40, C42, C43	Capacitor 0.01µF	Kemet	C0805C103K4RAC	11
C34	Capacitor 2.0nF	Kemet	C0805C202K5RAC	1
D1, D2, D3, D4	Shottky Diode	Motorola	BAT54WT1	4
L1	Inductor 1.8uH	Sumida	CEP1231R8MH	1
Q1, Q2	NMOS Transistor	NEC	uPA1707	1
Q3, Q4	NMOS Transistor	NEC	uPA1707	1
Q5, Q6, Q7, Q9, Q11,Q13	NMOS Transistor	Motorola	BSS123LT1	6
Q8, Q10	NMOS Transistor	Fairchild	HUF76131SK8	2
Q12	NPN Transistor	Motorola	MMBT2222A	1
R1, R47, R49	Resistor 10Ω, 5%	-	0805	3
R2, R3	Jumper 0Ω	-	0805	2
R4, R6, R15, R16, R18,R24, R25, R26, R27, R28, R32, R34, R37, R62	Resistor 10.0kΩ, 1%	-	0805	14

TABLE 2. BILL OF MATERIALS

REFERENCE	DESCRIPTION	VENDOR	PART NO.	QTY
R5	Resistor 3.57kΩ, 1%	-	0805	4
R7	Resistor 5.1Ω, 10%	-	0805	1
R8	Resistor 105kΩ, 1%	-	0805	1
R9	Resistor 75kΩ, 1%	-	0805	1
R10	Resistor 80.6Ω, 1%	-	0805	1
R11, R17, R51	Resistor 2.00kΩ, 1%	-	0805	3
R14, R60	Resistor 100kΩ, 1%	-	0805	2
R19	Resistor 7k50kΩ, 1%	-	0805	1
R20	Resistor 200Ω, 5%	-	0805	1
R21	Resistor 24.3kΩ, 1%	-	0805	1
R22, R23	Resistor 680Ω, 5%	-	0805	2
R29	Resistor 332kΩ, 1%	-	0805	1
R30	Resistor 110kΩ, 1%	-	0805	1
R31, R56	Resistor 25.5kΩ, 1%	-	0805	2
R33, R35	Resistor 9.09kΩ, 1%	-	0805	2
R38	Resistor 20kΩ, 1%	-	0805	1
R39, R42	Resistor 0.2Ω, 10%	Vishay	WSL2512	2
R40, R41, R43, R44	Resistor 0.1Ω, 10%	Vishay	WSL2512	4
R45, R46	Resistor 6.8Ω, 10%	Panasonic	P6.8WCT-ND	2
R55, R57, R59	Resistor 40.2kΩ, 1%	-	0805	3
R61	Resistor 23.2kΩ, 1%	-	0805	1
S1	Switch	E-Switch	KAL2104ER	1
SW1	Switch	E-Switch	KAL2110ER	1
TP1, TP2	Probe Socket	-		2
U1	Power Controller IC	Intersil Corp.	ISL6211	1
U2	Comparator	National	LMV331	1
U3, U15	Reference	National	LM4041DEM3-ADJ	2
U4, U6, U8, U9, U11	Timer	Intersil Corp.	ICM7555CBA	5
U5, U12, U13	Driver	Intersil Corp.	ICL7667SM	3
U7, U10	Multiplexer	TI	CD4053BCM	2
U14	Amplifier	National	LM358	2

Schematic Description

The evaluation board electrical schematic is presented in the Figures 1-3. The bill of materials is detailed in Table 2.

The DC-DC converter schematic is presented in Figure 1. The board layout is shown in Figures 9-14. The electrical components that comprise the evaluation board are arranged in several blocks that are outlined on the silk screen.

TABLE 3. S1 FUNCTIONALITY

SWITCH POSITION FROM THE LEFT	STATE (UP - CLOSED) (DOWN - OPEN)	FUNCTION
300kHz/600kHz	**Down**	300kHz
	Up	600kHz
FCCM#	**Down**	FCCM activated
	Up	Hysteretic Operation Enabled
Enable	**Down**	ISL6211 Disabled
	Up	ISL6211 Enabled
Load Emulator On/Off	**Down**	The Emulator is OFF
	Up	The Emulator is ON

The components that are directly related to the DC-DC converter are positioned in a square shaped envelope in the center-right part of the board. Those components include the PWM controller U1 ISL6211, MOSFETs Q2 and Q3, the filter inductor L1, and the output capacitors C10, C11, C12, and C5. Feedback and bias components are also located in this envelope.

The components, like dip-switches, signaling LEDs, jumpers, etc. that provide service functions and are not usually present in real applications, are positioned outside the converter envelope. The PLL power supply components U15, U16, Q6, Q12, etc. are assembled in the separate block outlined on the silk screen and marked CPU PLL. The load emulator components SW1, U4-U13, Q8, Q10, etc. are grouped in the L-shaped rectangular block located in the upper left portion of the board that is marked LOAD EMULATOR.

To provide maximum flexibility the evaluation board schematic has multiple positions for the most critical components like MOSFETs and output capacitors. The board can accommodate two MOSFETs for the upper switch and two MOSFETS for the lower switch. One pair of MOSFETs is positioned on the component side of the board. A second pair of MOSFETs can be placed on the bottom side of the board. Optional positions allow evaluation of different MOSFET combinations in the study of efficiency.

The output voltage is set by the dip-switch SW1 (Figure 1) by directly dialing appropriate VID codes. For START and DSX modes, the voltage is set by resistors R8 and R9, accordingly. In the simplest configuration only one 5V DC source is required to begin evaluation. The board can accommodate up to six surface mount, D-size electrolytic capacitors.

Two scope receptacles, TP1 and TP2, provide easy and convenient connection to observe PHASE and VOUT waveforms.

Power Connections

With the all supplies turned OFF, connect the 0-24V power supply positive terminal to the VIN post (J1) and the negative terminal to the nearest GND post (J3). Then connect the 0-5V power supply positive terminal to the VCC post (J4) and the negative terminal to the nearest GND post (J2).

In the minimal configuration only one 0-5V supply can be used. In this case, connect the VIN post to the VCC post with a jump wire.

NOTE: Do not forget to remove this wire when proceeding to tests with voltages higher than 5V! Not removing the wire can permanently destroy the IC if high voltage is applied to the VCC pin.

Connect the electronic load positive terminal to the V_CORE posts (J5, J6) and the negative terminal to GND posts (J7, J8).

In the minimal configuration the internal LOAD EMULATOR can be used. Put the ‘Load On/Off’ switch of the S1 switch assembly in the upper position and close the JP4 jumper to activate the emulator.

Performance Characterization

This section shows captured performance data from a standard bench setup. It will include descriptions of the experiments performed and the conditions applied.

Switching Frequency

The ISL6211 PWM controller can operate on either 300kHz, or 600kHz switching frequency. The frequency can be changed by switching the S1 switch. The lower position sets the lower switching frequency, and the higher position sets the higher frequency. If not otherwise stated, the measurements in this application note are made with the 300kHz switching frequency.

Soft-Start

In a start up event, the IC is ramping-up the output voltage smoothly to the programmed level by following voltage on the SOFT pin. During voltage ramp-up, the under-voltage and PGOOD signals are disabled until the output has risen to within 75% of its target. Only then are the protections enabled and PGOOD is released to be reported.

Figure 4 shows the output voltage response to the application of supply voltages and the EN signal. The scope is set to trigger in a single-shot mode on EN going high.

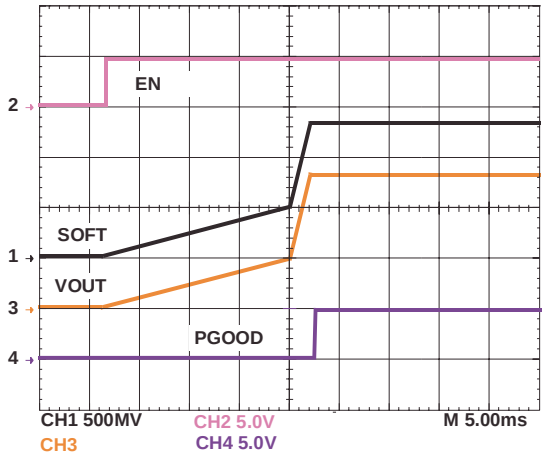

FIGURE 4. INITIAL START UP

Steady-State Operation

Depending on the load level and the control signals applied, ISL6211 can operate either in continuous conduction (CCM), or discontinuous hysteretic mode. The CCM mode is usually associated with higher currents. Output and the phase node waveforms for both modes of operation are presented in Figures 5 and 6.

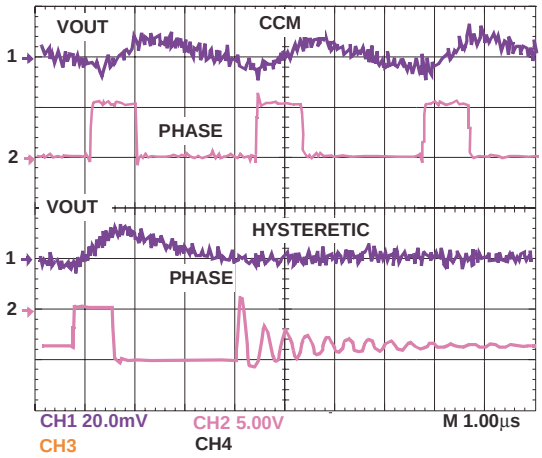

FIGURE 5. SWITCHING AND RIPPLE WAVEFORMS Vin = 5.0V

To observe the waveforms shown in Figures 5 and 6, place the scope probes into the receptacles TP1 and TP2. Enable the hysteretic mode of operation by putting the FCCM switch (S1) in the high position. Synchronize the scope to the channel connected to the TP1 (PHASE) test point.

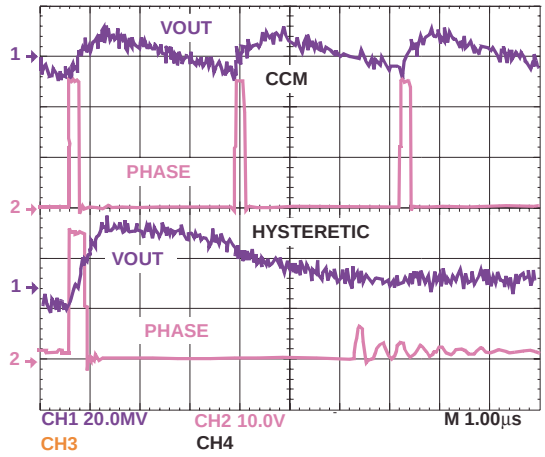

FIGURE 6. SWITCHING AND RIPPLE WAVEFORMS Vin = 10.0V

Adaptive Voltage Positioning

To reduce the size of the output filter, an adaptive voltage positioning is used in the CPU power applications. The technique is based on lowering the output voltage as the load increases.

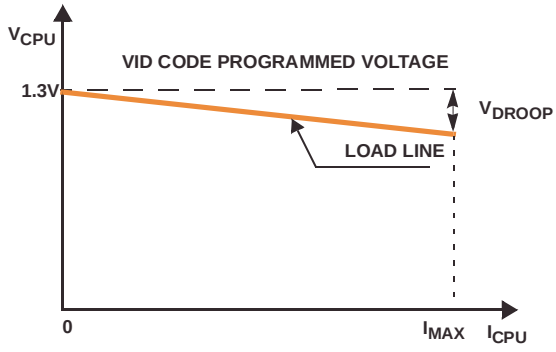

FIGURE 7. OUTPUT VOLTAGE DROOP

The output voltage varies with the load as if a resistor were connected in series with the converter's output, as it is shown in Figure 7. When done as a part of the feedback in a closed loop, the output voltage droop is not associated with substantial power losses, because the feature is emulated by the feedback.

The output voltage variation for the TM5800 CPU is specified as +5%/-2% of the set voltage. The recommended use of the allowed regulation window is presented in Figure 8. The maximum allowed ripple is assumed to be no more than 2% of the nominal output voltage determined by the VID code, or potential on the ALTV pin. The 1% safe margins on both sides of the regulation window provide required guard toward components tolerance.

With assumed ripple and margins, the initial voltage rise and droop value are about 3%.

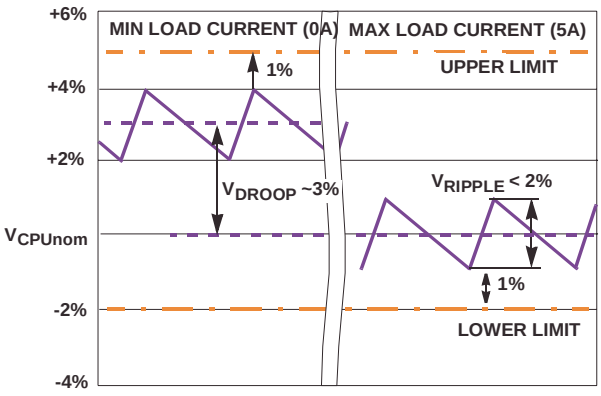

FIGURE 8. ADAPTIVE VOLTAGE POSITIONING

Transient Response

The converter response to the load step of 5A is shown in Figure 9. At zero load current, the output voltage is raised ~40mV above nominal value of 1.30V. When the load current increases to its maximum value, the output voltage drops down. Due to the use of droop, the converter's output voltage adaptively changes with the load current allowing better utilization of the regulation window.

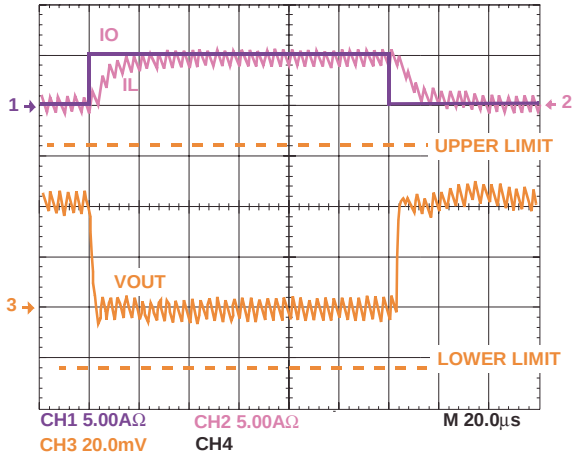

FIGURE 9. TRANSIENT RESPONSE TO THE LOAD STEP 0A...5A

Auxiliary Over-Voltage Protection Circuit

While evaluating a new platform, mistakes and mishaps are almost inevitable. The TM5800 family CPUs have maximum operating voltage VCPU = 1.4V and can be easily damaged by applying a wrong VID code for a long time. To protect a valuable CPU from being destroyed during evaluation, an external over-voltage circuit is incorporated in the evaluation board as an extra protection and convenience measure. The circuit consists of the reference voltage source U3 and the comparator U2. The divider R19/R21 sets the reference voltage to a desired level. The circuit is engaged when jumper JP3 is closed.

When engaged, the over-voltage circuit limits the SOFT voltage to the level predetermined by the reference source.

CPU Emulator

To simplify the task of core regulator supply evaluation, the board is equipped with a CPU emulator. The emulator applies control signals and VID codes to the converter in a repeatable manner actively changing its operating modes. The output voltage and the load current is shown in Figure 10. The electrical schematic of the converter is presented in Figure 2.

The square wave generator U4 generates the DSX signal that is applied to the gate of Q2. When the DSX signal is high it commands the converter into DSX mode. The output voltage is programmed by the resistor R9 and the VID code is disregarded. When the DSX signal is low, operation using VID codes is enabled. Just after the DSX turns from high to low, the START signal is generated by single-shot U11.

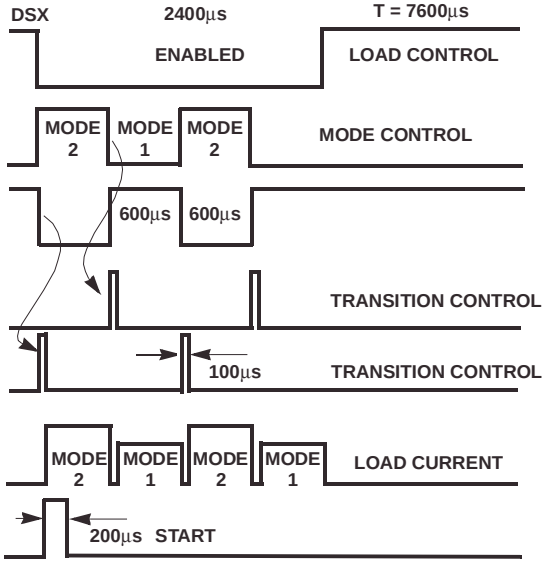

FIGURE 10. CPU EMULATOR TIME DIAGRAM

The START signal is applied to the gate of Q5 and programs the output voltage by the resistor R8. In the START mode the VID code is rejected. While DSX stays low, the multi-stable generator with 50% duty-factor U6 changes its output from high to low and backwards for several cycles. The MODE CONTROL signal is applied to two multiplexers U7 and U10 that are connected to the VID lines of the controller and switch between two VID codes dialed by SW1. The low MODE CONTROL signal is associated with MODE1, which usually has a lower CPU voltage. The high MODE CONTROL signal is, correspondingly, associated with the higher output voltage mode, MODE 2. As the MODE CONTROL signal changes its state, Q8 and Q10 apply load resistors R39...R44 to the converters output. The resistors' values are chosen to coordinate with current loading that a real CPU would produce. The CPU leakage current is represented by R45 and R46.

To achieve a higher degree of resemblance of the waveforms produced by the load emulator, the load is reduced to the leakage level during LongRun™ transitions as it would happen with a real CPU. This is done by two one-shots U8 and U9 that generate short pulses every time the mode changes. These pulses turn off Q8 and Q10, which in turn disconnect loading resistors from the converter output. The time interval during which load is disconnected can be matched to the LongRun™ transition time by changing the time constant of the circuits R33/C24 and R35/C26.

The output waveform generated by the converter with activated CPU emulator is shown in Figure 11.

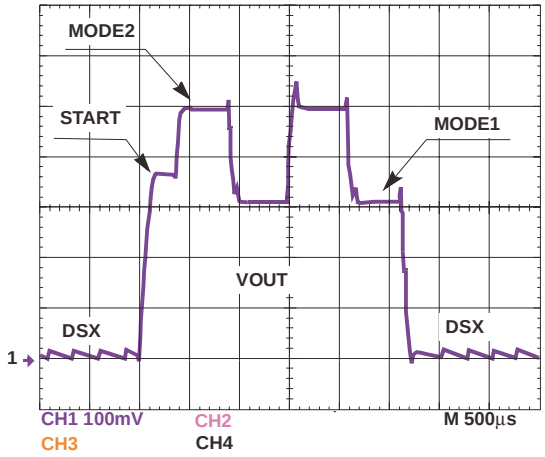

FIGURE 11. CONVERTER WAVEFORM WITH LOAD EMULATOR

Efficiency

Efficiency curves captured at different input voltages with the output voltage Vo = 1.3V are captured in Figure 12.

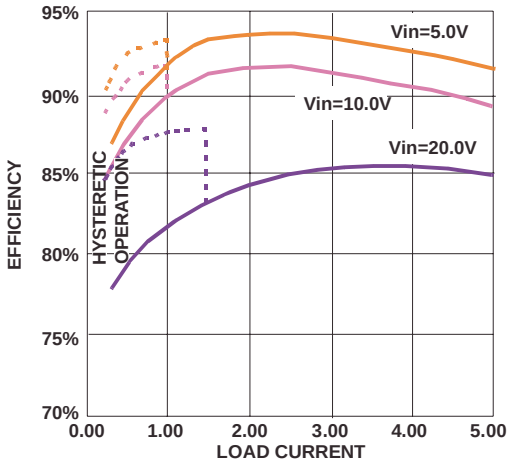

FIGURE 12. ISL6211 EFFICIENCY

The efficiency curves are captured with and without hysteretic mode enabled in light loads. The dashed lines show efficiency improvement when the hysteretic mode of operation is enabled.

NOTE: When measuring efficiency, do not forget to turn off the CPU emulator and open the jumper JP4. To measure current consumed by the control IC and the gate drive circuitry, open the jumper JP1 and place ampere-meter across the jumper posts.

PLL Supply

The TM5500...TM5800 processors require that V_CPU_PLL track the core voltage within ±50mV down to the lower boundary of 1.0V. As the core voltage drops lower than 1.0V, the V_CPU_PLL must remain at 1.0V. During LongRun transitions, V_CPU_PLL must settle to within the ±50mV of V_CPU_CORE voltage in 25µs. Figure 13 graphically shows this requirement.

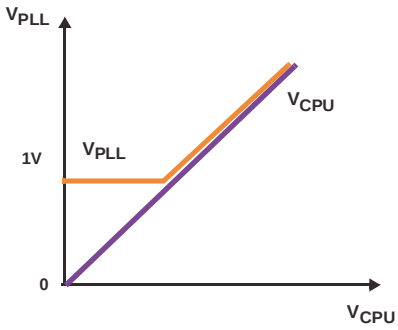

FIGURE 13. PLL SUPPLY OUTPUT CHARACTERISTIC

The schematic in Figure 3 depicts the circuit that provides the required tracking function. The circuit includes the enable switch Q13; the reference voltage source U15, R51, R56, and R57; the 'ideal' diode U14a and D6; and the output buffer U14b and Q12. The R55/R59 divider creates a 1.0V reference for the minimum V_CPU_PLL operating voltage that is applied to the positive input of the error amplifier U14a with a diode in its feedback. The negative input of U14a will be regulated to the voltage on its positive input due to high gain of the amplifier. Due to the diode D6 in the feedback path of U14a the regulation will be achieved only if the core voltage is lower than the voltage on R59. For core voltages higher than 1.0V, the diode D6 will be blocked and the voltage on the negative input of U14a will follow the V_CPU_CORE via R53. The voltage follower U14b and Q12 provides the required current capability for the PLL supply and circuits separation. The circuit is enabled by connecting the Q13 gate to the CPU regulator PGOOD signal.

Considering ±50mV tolerance requirements, the PLL circuit can be significantly simplified by eliminating the reference source U15. The 1.0V voltage on the resistor R59 should be derived from any system voltage available. The emitter follower Q12 can also be eliminated if V_CPU_PLL current requirements fall within the amplifier loading capabilities. Check the CPU data sheet and Transmeta design guidelines for updates.

Typical Application Circuit

The typical application circuit to be populated in custom designs is presented in Figure 14.

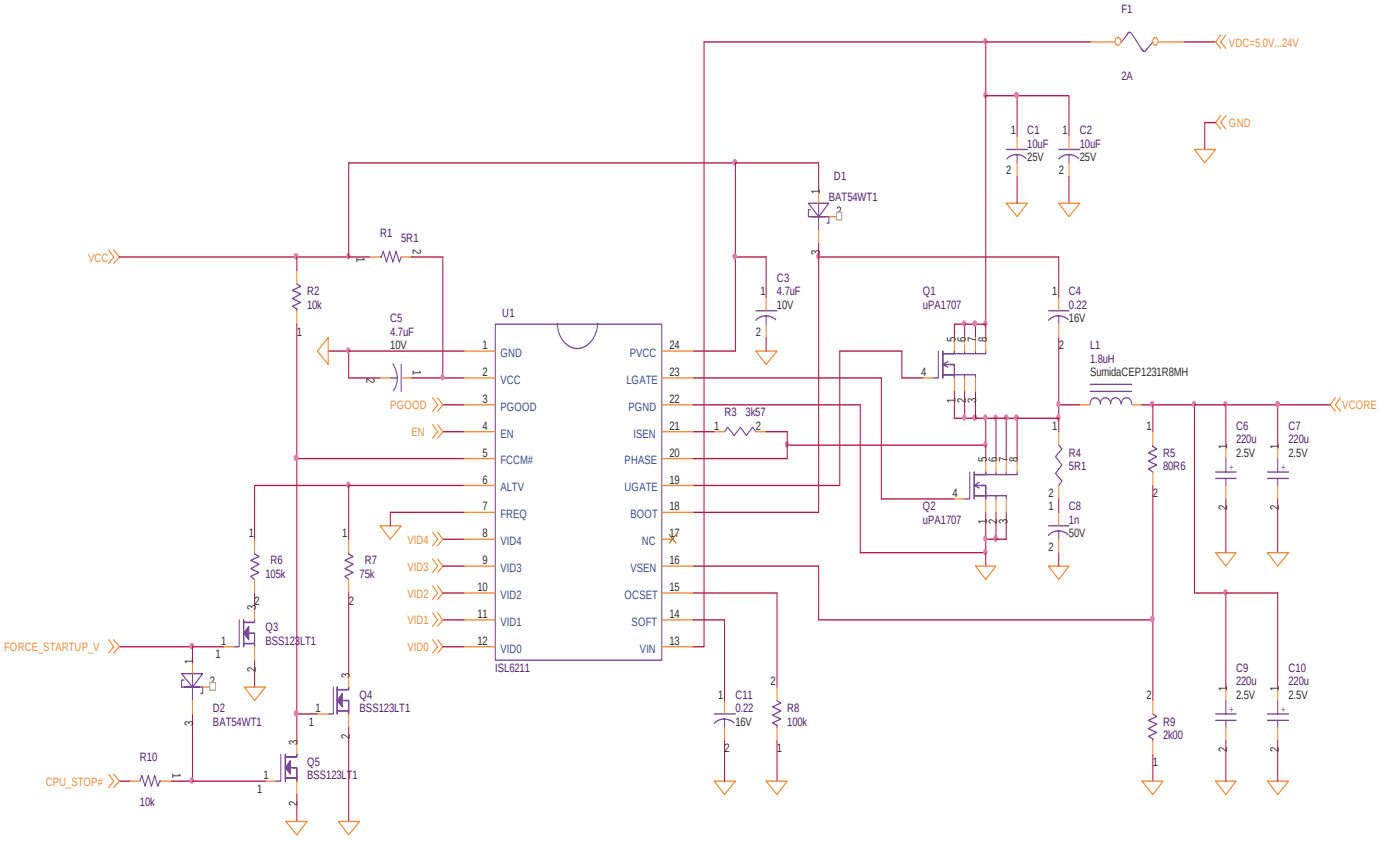

FIGURE 14. PRACTICAL POWER SUPPLY DESIGN FOR TM5800 CPU

ISL6211 EVAL2 Layout

Drawings of the evaluation board layout, by layer,

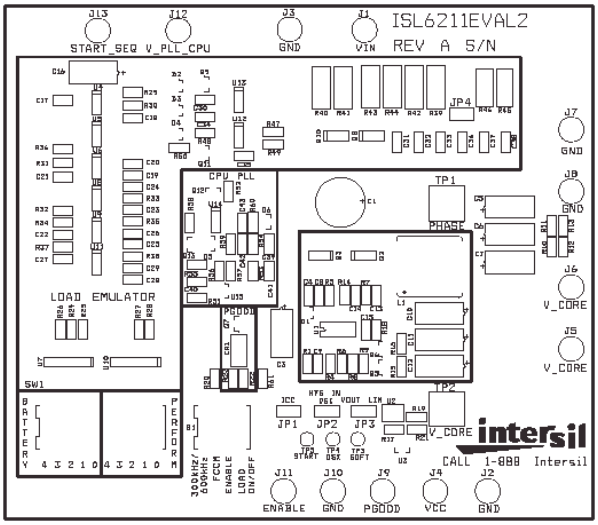

FIGURE 15. TOP SILK LAYER

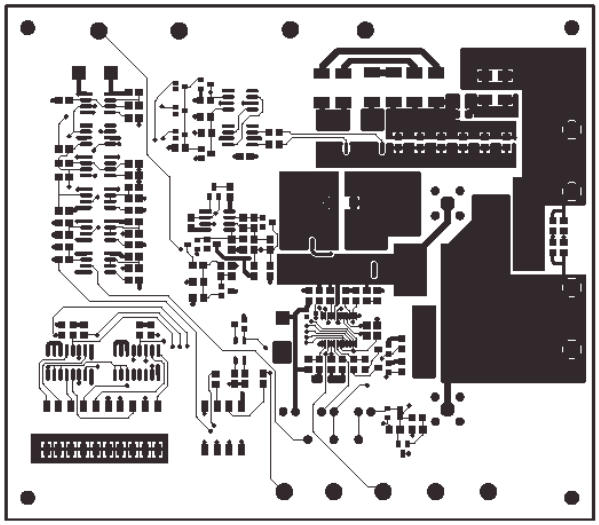

FIGURE 16. TOP WIRE LAYER

ISL6211 EVAL2 Layout Drawings of the evaluation board layout, by layer, **(Continued)**

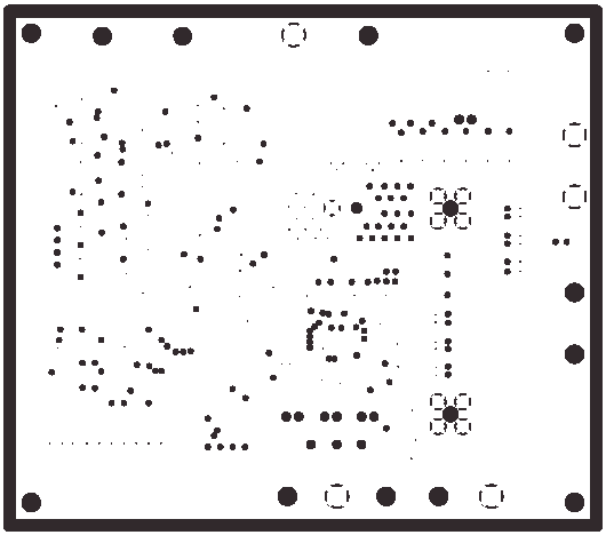

FIGURE 17. GROUND LAYERS

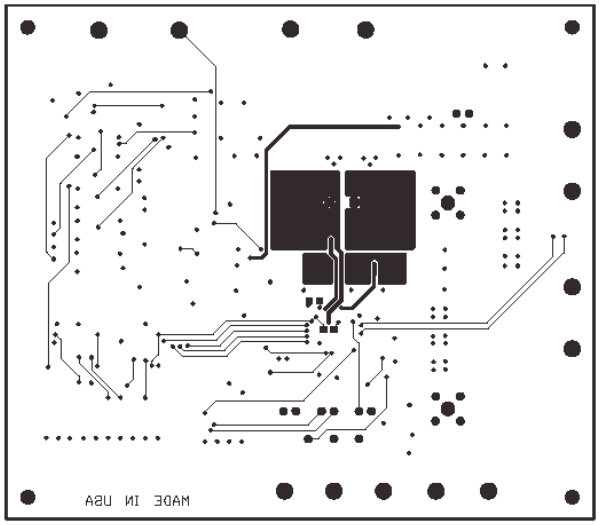

FIGURE 18. BOTTOM WIRE LAYER

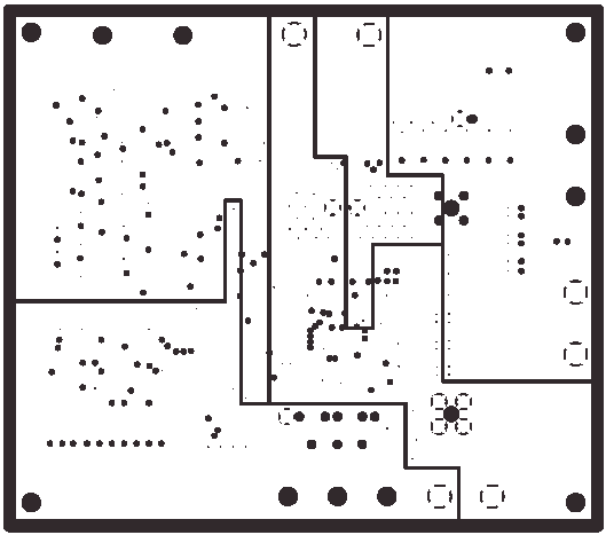

FIGURE 19. POWER LAYERS 1&2

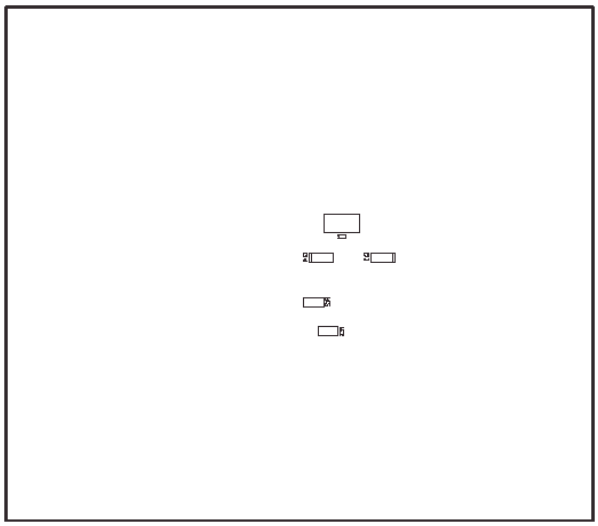

FIGURE 20. BOTTOM SILK LAYER

References

Intersil documents are available on the web at http://www.intersil.com.

[1] ISL6211 Data Sheet, Intersil Corporation, File No. FN9043.

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